REMARKS

We are in receipt of the Office Action of August 29, 2001, and the accompanying amendments and remarks are made in light thereof.

In the Office Action, objection is made to the title of the invention; claims 11-14 are rejected under 35 USC 102(b) as being anticipated by Belscher et al., U.S. Patent No. 5,792,327; and claims 15-30 are rejected under 35 USC 103(a) as being unpatentable over Kobayashi et al., U.S. Patent No. 5,102,813 in view of Mautz et al., U.S. Patent No. 5,476,816.

With respect to the title of the invention, the title has been amended to read as indicated above.

Turning to the rejections based upon prior art, the present invention is characterized by the removal of impurities in an interface between a semiconductor film and a gate insulating film or in an interface between the gate insulating film and a gate wiring by spin etching. The impurity is such as alkaline metals and alkaline earth metals. Please see page 2, line 5 to line 13. Such an impurity in the interface between the semiconductor film and the gate insulating film or in the interface between the gate insulating film and the gate wiring is a major detriment to TFT reliability. See an example of the TFT reliability that is shown in Figs. 4 to 6 and page 4, line 5 to page 5, line 1 in the specification in which sodium (Na) exists in the interface between a gate wiring and a gate insulating film.

With respect to the 102(b) rejection, Belscher et al. disclose chemically treating a surface of a glass to improve adherence of a metal film and the glass substrate. Claim 11 has been amended to overcome the rejection.

With respect to the 103(a) rejection, Kobayashi et al. disclose a method of manufacturing a thin film transistor as shown in Fig. 7. Further, Mautz et al. disclose cleaning a first interlevel insulating layer and a second interlevel insulating layer by an acid-compatible spray tool which is similar to a spin rinse dryer after a plasma metal etching step.

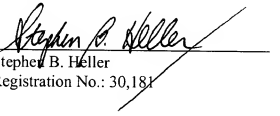
Mautz et al. do not disclose the present invention, i.e., removing impurity in an interface between a semiconductor film and a gate insulating film or in an interface between a semiconductor film and a gate insulating film or in an interface between the gate insulating film and a gate wiring.

Applicant believes that, in view of the improvement in TFT reliability, the present invention is more effective than Mautz et al. because the gate insulating film of the present invention is closer to the semiconductor film than the first or second interlevel insulating layer of Mautz et al.. The closer to the semiconductor film a film that has impurity is, the more the impurity has effect on the electrical property of TFT.

Further, Kobayashi et al. do not disclose the present invention, i.e., removing impurity in an interface between a semiconductor film and a gate insulating film or in an interface between the gate insulating film and a gate wiring.

For all of the above reasons, Applicants respectfully submit that the pending claims are patentable over the art of record. Accordingly, reconsideration and allowance of such claims are respectfully requested.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE:

Please change the title of the application to [SEMICONDUCTOR DEVICE AND] A METHOD OF MANUFACTURING [THE SAME] A SEMICONDUCTOR DEVICE.

IN THE CLAIMS:

Please amend claims 11, 15 and 23 as follows:

11 (Amended). A method of manufacturing a semiconductor device, comprising steps of:

forming a [first] semiconductor film;

removing a contaminating impurity from the surface of the [first] semiconductor film; and

forming a [second] gate insulating film in contact with the [first] semiconductor film from the surface of which the contaminating impurity has been removed.

15 (Amended). A method of manufacturing a semiconductor device, comprising steps of:

forming at least one semiconductor island over a substrate;

spinning the substrate by using a spinning apparatus;

contacting an etching solution to a surface of said semiconductor island and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface; and then

forming [an] a gate insulating film over said semiconductor island.

23 (Amended). A method of manufacturing a semiconductor device, comprising steps of:

forming gate wirings over a substrate;

spinning the substrate by using a spinning apparatus;

contacting an etching solution to surfaces of said substrate and said gate wirings and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surfaces; and then

forming [an] a gate insulating film and a semiconductor film over said gate wirings.